University of Thi -Qar Journal for Engineering Sciences
http://www.doi.org/10.31663/tqujes.12.2.454(2022)
Vol 12.2(December 2022)

ISSN :2664- 5572 (online)
ISSN:2664-5564 (print)
Available at http://jeng.utq.edu.iq
utjeng@ utq.edu.iq

Improved CMOS realizations of active inductor for RF applications

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Abstract
Many Radio frequency circuits such as low noise amplifiers, voltage-controlled oscillators, and RF filters need inductors for realization. Passive and spiral implementations of the inductors have many limitations precisely when these RF circuits are designed and realized as integrated circuits. Typically, standard structure realized active inductors provide a limited inductor value and quality factor. This paper presents an alternative active Complementary Metal-Oxide Semiconductor realization based on the use of a gyrator-c configuration that is suitable for integrated circuit fabrication. A comparative study between various active inductor realization topologies is performed to obtain and improve active inductor performance. The most important parameters that have to be investigated are the quality factor, the range of inductors value at the specified operating frequency, and the self-resonant frequency. It is shown that the use of passive feedback improves active inductor performance, however large passive resistance is required that is not suitable for IC fabrication. An alternative MOS transistor and voltage divider structures are used to replace the passive feedback resistor that improves performance without requiring a large chip area for fabrication. It is also shown that different transistor dimensions and current source values result in different performance parameters. Therefore, minimized transistors dimensions are required for minimum chip area, and also minimized current values are required to minimize power consumption. It is shown that the voltage divider AI realization resulted in a significant improvement in inductance value (L=20.16 nH) and higher quality factor (Q=3.078) compared to other topologies.

Keywords—Active inductor, CMOS RF application, Integrated CMOS realization.

1. Introduction

Inductors are usually treated as critical components in the design of RF circuits. Filters, low-noise amplifiers, mixers, and voltage controlled oscillators all require inductors. However, analog integrated circuit design must maximize inductance, quality factor, and self-resonant frequency in order to minimize chip space, cost, and power consumption. Passive (Spiral) and active structure are the two approaches to inductor realization. **[1]**.CMOS active inductors have a small chip area, a high-quality factor, a large inductance, and a high self-resonant frequency. However passive inductors provide a low-quality factor, a small inductance values, low self-resonant frequency, and a large chip area **[2]**. Typically, active inductors are constructed using a gyrator design, in which two transistors are coupled back to back. **[3]**

A gyrator-C structure is employed to realize active inductors as illustrated in fig(1).

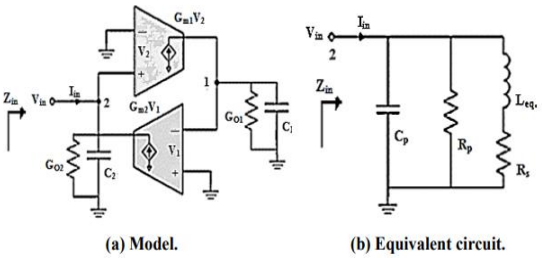

Fig.1 The Gyrator-C active inductor topology.

Figures 1 (a) and (b) present the general gyrator-C lossy active inductor and its equivalent circuit. The lossy parameter exists because of the non-zero input and output impedances of the circuits, but have an infinite values. The equivalent circuit in figure (1) includes parasitic elements a (C1,2, G01, and G02) , these parasitic limit the frequency range of operation of simulated inductors. The gyrator-C topology input admittance looking into port 2 may be derived using circuit analysis and it is given by the Eqs. (1) to (6) **[2]**

$$Y_{in} = \frac{1}{Z_{in}} = \frac{I_{in}}{V_{in}} = SC_2 + G_{O2} + \frac{1}{S\left(\frac{C_1}{G_{m1}G_{M2}}\right)+\left(\frac{G_{O1}}{G_{m1}G_{m2}}\right)} \quad (1)$$

Equation (1) can be represented and modeled by an RLC network that is shown in Fig. 1(b), where:

$$R_p = \frac{1}{G_{O2}} \quad (2)$$

$$R_S = \frac{G_{O1}}{G_{m1}G_{m2}} \quad (3)$$

$$C_P = C_2 \quad (4)$$

$$L_{eq} = \frac{C_1}{G_{m1}G_{m2}} \quad (5)$$

As a result of the presence of these parasitic, lossy inductor behavior occurs. As a result, the most important condition for approaching perfect behavior is to eliminate or reduce these parasites. Because of the existence of parasitic parallel resistance (R_p), parallel capacitance (C_p), and series resistance (R_s), the Gyrator-C network acts similarly to a lossy inductor. To minimize the ohmic loss, maximization of R_p and minimization of R_s should be considered. However, the value of active inductor's is unaffected by the finite input and output impedances of the trans conductors in the gyrator-C network (AI). The self-

resonant frequency (SRF) of this active inductor is given by **[2, 4]**

$$W_o = \frac{1}{\sqrt{LC_P}} = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} \quad (6)$$

This paper presents a comparative study for various AI realization topologies. A modified structure are designed and realized to improve the active inductor performance.

2. Active Inductor realization topologies

There are many structures that realize the active inductor. The following topologies have different performance:

2.1 Basic active inductor

The positive trans conductance is achieved by configuring transistor M_2 as a common drain as shown in fig (2). In a common source arrangement, M_1 realizes the negative trans conductance. M_1 and M_2 must be biased to operate in active region using two current sources I_1 and I_2 in addition to supply voltage V_{DD}. The performing of small signal analysis results in to an equivalent inductance and equivalent quality factor for the grounded inductor that are given in Eqs. (7) and (8). **[5]**

$$L = \frac{C_{gs1}}{g_{m1}g_{m2}} \quad (7)$$

$$Q = \frac{g_{m2}C_{gs1}}{g_{m1}C_{gs2}} \quad (8)$$

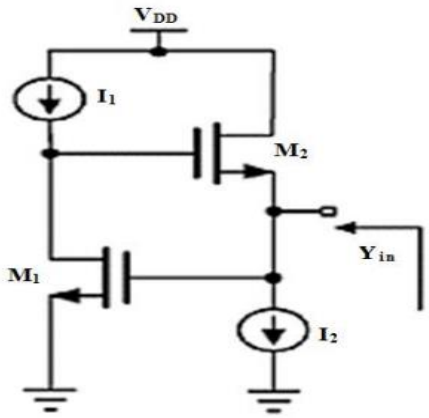

Fig.2 Schematic diagram of basic active inductor.

Moreover, the self-resonance frequency (SRF) can be written as in Eq. (9).

$$SRF = \sqrt{\frac{1}{C_P L_{eq}}} = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \quad (9)$$

The total power consumption is therefore given by Eq. (10)

$$P = (I_1+I_2)V_{DD} \quad (10)$$

2.2 Feedback resistor active inductor

A passive resistance R_f is added that acts as negative feedback as shown in fig. (3) to improve active inductor performance and to decrease its sensitivity. The value of inductance and quality factor are given as :

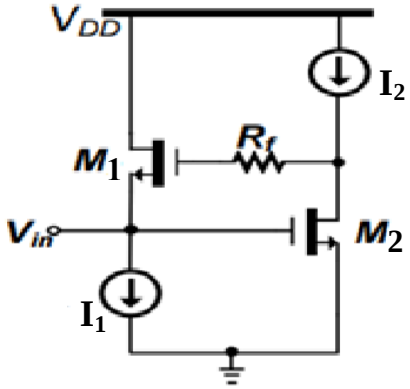

Fig.3 Schematic diagram of feedback resistor active inductor.

$$G = g_{ds2} + \frac{g_{m1}}{1+R_F g_{ds1}} \quad (11)$$

$$L = \frac{C_{ds2}(1+R_f g_{ds1})}{g_{m1}g_{m2}} \quad (12)$$

$$Q = \frac{g_{m2}C_{gs1}(1+R_F gds_1)}{g_{m1}C_{gs2}} \quad (13)$$

Eq. (11, 12, and 13) illustrates the effect of the factor R_f, and it is selected to have a value greater than unity. This resulted equivalent conductance loss (G) is to be minimized, as well as an increasing of the equivalent inductance (L) by ($I+ R_f g_{ds1}$) factor**[6]**.

To preserve the advantages of applying a negative feedback, while avoiding the use of passive resistance. An alternative modified active realizations is next considered.

2.3 Active inductor with feedback transistor

A new realization that based on the use of negative feedback element by utilizing active transistor (M_3) is presented in fig. (4). The inductance value and quality factor are significantly improved. The MOS transistor M_3 behaves as resistance with the value given by:

$$Ron = \frac{L}{K'W(V_{GS}-V_T-V_{DS})} \quad (14)$$

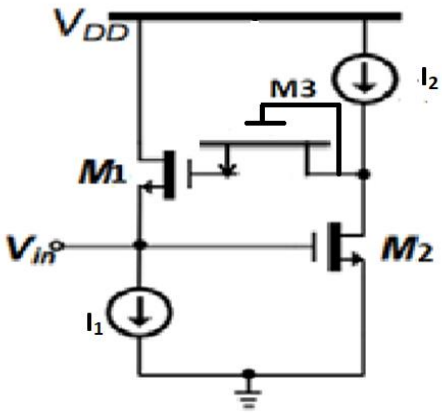

Fig.4 Schematic diagram of Active inductor with feedback transistor M_3.

2.4 Active inductor with feedback voltage divider

Another modified structure is illustrated in fig. (5) that utilizes variable gate voltage on feedback transistor (M_3). The voltage divider is applied to control the gate voltage, therefore controlling the ON resistance of the feedback transistor M3.

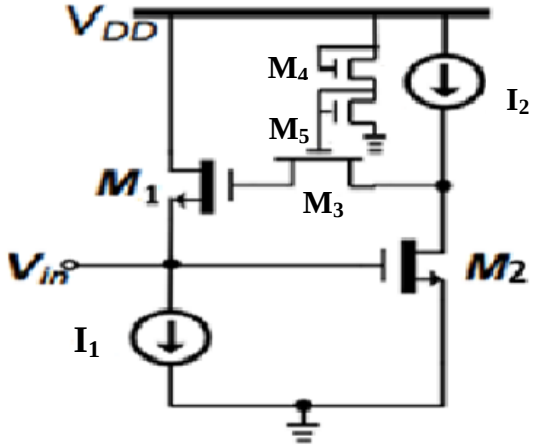

Fig.5 Schematic diagram of active inductor with feedback voltage divider.

$$V_G = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4+\left(\frac{W}{L}\right)_5} V_{DD} \qquad (15)$$

3. Design and simulation of Active Inductor

The design of an active inductor for a 2.4 GHz RF application is presented. The design is based on the use of a 0.18 µm process to implement various active inductor circuits. As presented previously, the active inductor values and its quality factor are determined by MOS transistors dimension and the values of current sources. Table (1) and table (2) illustrate the active inductor performance parameters as a function of the design parameters values. Therefore a proper selection of these design parameters is an important issue to obtain a realization that provide required performance with suitable technological limitations.

Advanced Design System (ADS) simulation software is applied to simulate the different active realization topologies ADS includes various analysis such as circuit analysis, circuit layout, and other simulation, analysis. ADS is the world's most popular electronic design automation software for applications such as radio frequency, microwave, high-speed digital, and power electronics **[7].** The simulation results are for the two deigns in consideration are presented in fig. (6) and fig. (7) for the first design and in fig. (8) and fig.(9) for the second design.

Table 1 Active Inductor performance parameters of design 1.

parameters	Basic (A)	Resistor feedback (B)	Transistor feedback (C)	Voltage divider (D)
F (GHz)	2.4	2.4	2.4	2.4
W_1 (µm)	5	5	5	5
W_2 (µm)	1	1	1	1
W_3 (µm)	∞	∞	1	4
W_4 (µm)	∞	∞	∞	8
W_5 (µm)	∞	∞	∞	4
R_F	∞	10000	∞	∞
I_1 (mA)	0.25	0.25	0.25	0.25
I_2 (mA)	0.1	0.1	0.1	0.1
L (nH)	4.647	5.267	8.891	13.48
Q	2.274	3.768	1.091	3.728

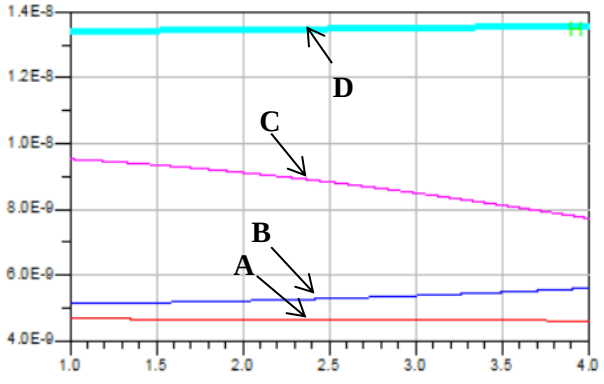

Fig.6 Inductance values for (A) Basic structure, (B) Resistor feedback structure, (C) Transistor feedback structure, (D) Voltage divider structure for design1.

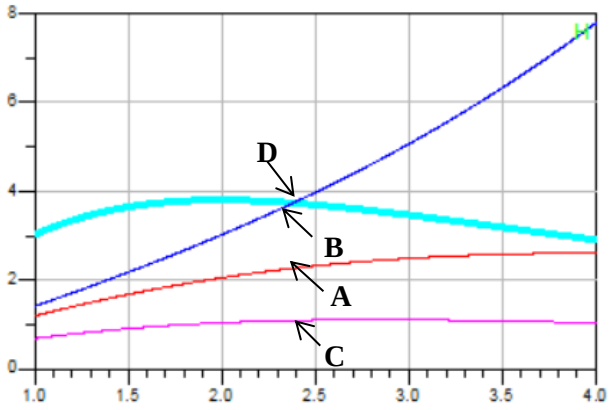

Fig.7 Quality factor values for (A) Basic structure, (B) Resistor feedback structure, (C) Transistor feedback structure, (D) Voltage divider structure for design 1.

Table 2 Active Inductor performance parameters of design 2.

parameters	Basic (A)	Resistor feedback (B)	Transistor feedback (C)	Voltage divider (D)
F (GHz)	2.4	2.4	2.4	2.4
W_1 (µm)	12	12	12	12
W_2 (µm)	1	1	1	1
W_3 (µm)	∞	∞	1.5	5
W_4 (µm)	∞	∞	∞	8
W_5 (µm)	∞	∞	∞	4
R_F	∞	10000	∞	∞
I_1 (mA)	0.1	0.1	0.1	0.1
I_2 (mA)	0.15	0.15	0.15	0.15
L (nH)	8.573	9.679	15.07	20.16
Q	3.332	10.512	1.447	3.078

Figure 6 and figure 7 illustrate that voltage divider topology has greater inductance and range and higher quality factor compared with the other structure.

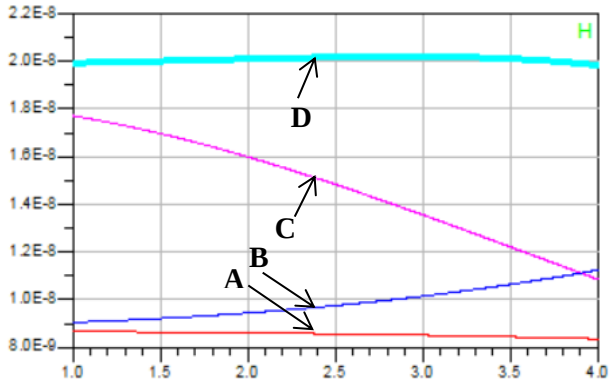

Fig.8 Inductance values for (A) Basic structure, (B) Resistor feedback structure, (C) Transistor feedback structure, (D) Voltage divider structure for design 2.

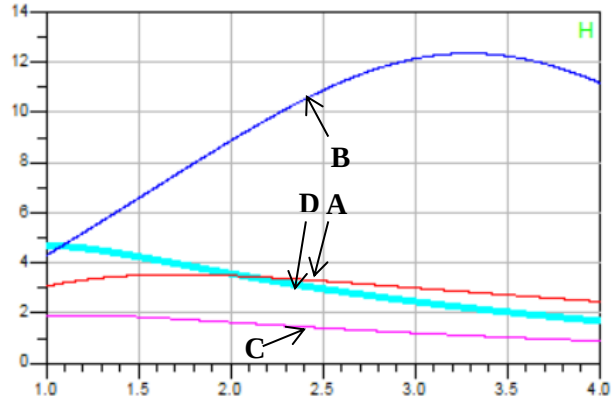

Fig.9 Quality factor values for (A) Basic structure, (B) Resistor feedback structure, (C) Transistor feedback structure, (D) Voltage divider structure for design 2.

It can be seen from the above figures that a significant increase in quality factor of the active inductor is obtained by using the feedback transistor and the voltage divider structures with acceptable values of realized inductance values. Also, it is clear that all structures provide nearly constant inductance values over a wide range of operating frequency.

Conclusions

An active CMOS realizations based on gyrator-C technique was presented in this paper. Basic topology, feedback resistor structure, MOS transistor feedback realization, and the voltage divider structure were realized, designed, and simulated. A comparison between these topologies was accomplished from point of view of active inductor performance parameters that include the inductance value and the quality factor.

An Advanced design System (ADS) simulation method were used to verify the operation of AI and to compare between the performance of these topologies.

It was proved that the modified topologies by utilizing MOS transistor structure, and voltage divider topology resulted in a significant improvement in active inductor performance. These modified structures provide

(L=15.07nH, Q=1.447) and (L=20.16nH, Q=3.078) for MOS transistor and voltage divider topologies respectively. The price of this improvement is extra devices which means a larger fabrication area.

It was illustrated from table 1 and table 2, that a proper selection of different design parameter values resulted in different performance parameters for each topology individually, therefore a genetic algorithm (GA) optimization approach as future work is to be applied to minimize chip area and minimize power consumption.

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